Tracking capability of intermediate + thiner outer tracker

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sPHENIX tracker meeting, June 17, 2016

Introduction and motivation

- We investigate how the silicon-strip intermediate tracker can improve the overall detector performance:
  - combination of the intermediate- and thiner outer-tracker [today's talk]
  - track recognition in a large pileup probability [before tracker review]

- Intermediate and thiner outer tracker combination aims at tracking capability requested by the sPHENIX science drivers by keeping the building cost as low as possible.

Tracker overview

- ***Inner tracker***
  - one layer of VTX pixel with 100 % live area: R = 2.48 cm
  (because this study was done before submitting ALD charge.)

- ***Intermediate tracker***
  - four layers of silicon-strip detectors: R = 6, 8, 10, 12 cm
  - one strip corresponds to 80 μm (φ) x 12 mm (z)
  - one chip per one cell, so no strip ganging.

- ***Outer tracker***
  - a chamber consisting of six pads/layers placed at R = 77.5, 79.0, 80.5, 82.0, 83.5, and 85.0 cm.

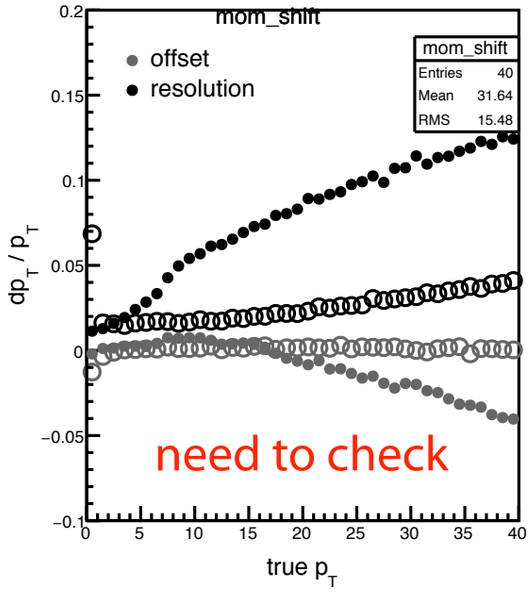
Simulation methodology

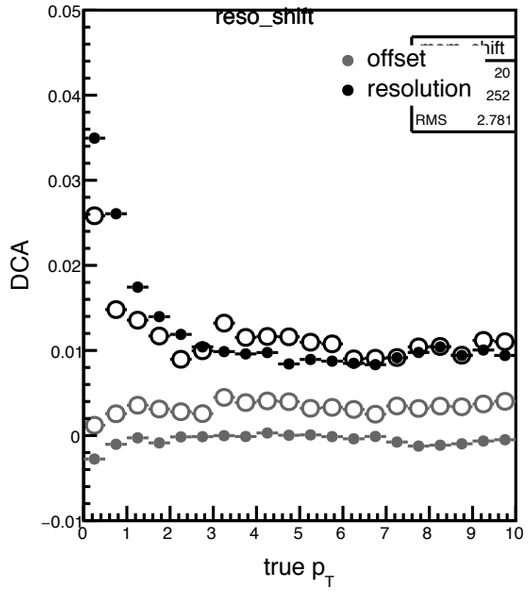
- sPHENIX Geant4 is used ("toy MC" is not used anywhere in this report.)
- Implementation of VTX pixel and silicon-strip sensors use the "cylinder geometry templates" in G4_Svtx.C.
- For a thiner outer tracker, I first tried to modify the TPC configuration, but finally I used the silicon-strip template with the strip width equivalent to the position resolution (here I assume 250 μm) and strip length 1.2 cm (with no special reason).
- PHG4HoughTransform, not PHG4HoughTransformTPC, is used for track reconstruction.
- Currently a track must have hits in totally 11 layers from VTX pixel to the most outer layer in the outer tracker. Note that the track efficiency/purity is sensitive to this requirement.

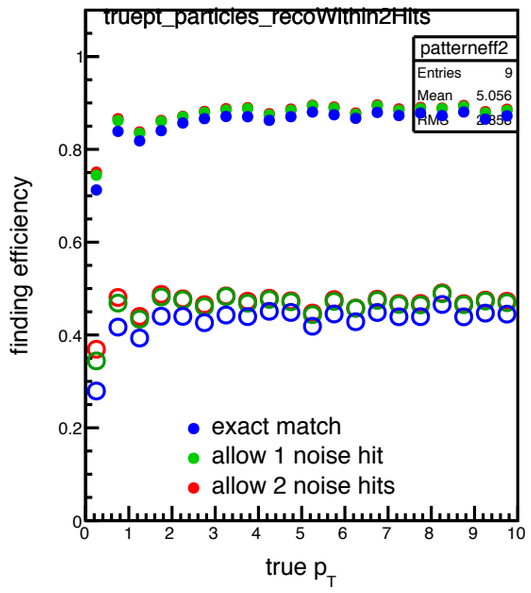
Tracking performance

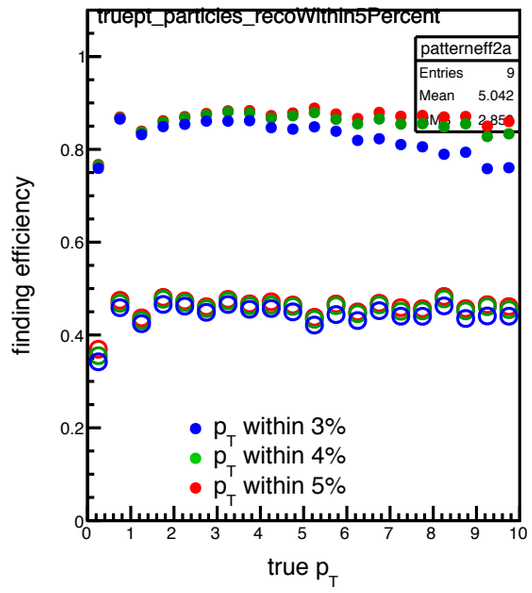
(PHG4 with 20,000 HIJING events at b < 4 fm)

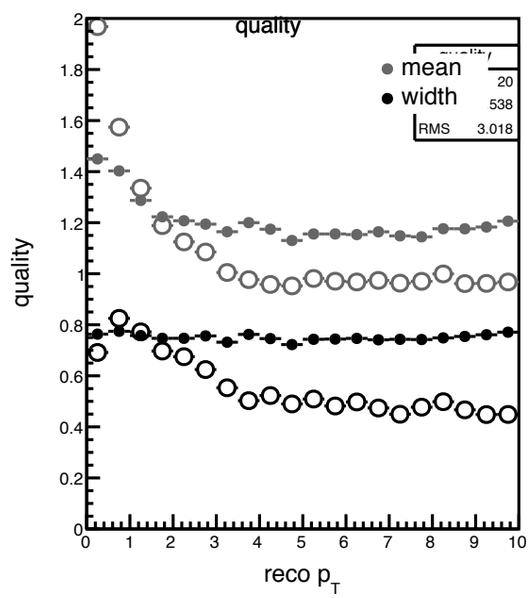
Open circles: silicon option in pCDR
Filled circles: this option (VTXP+intermediate silicon+thiner outer)

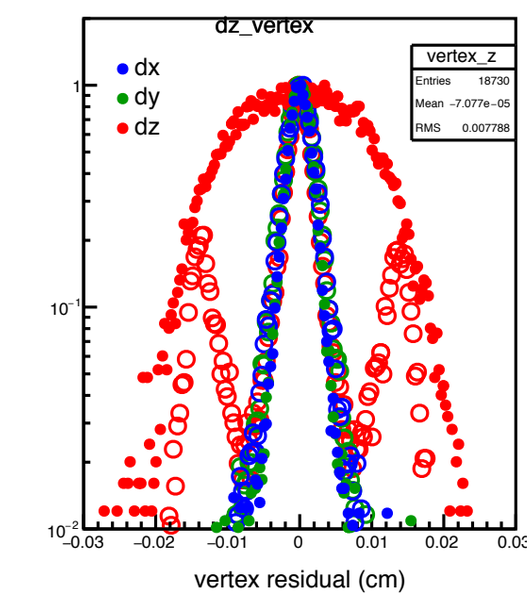


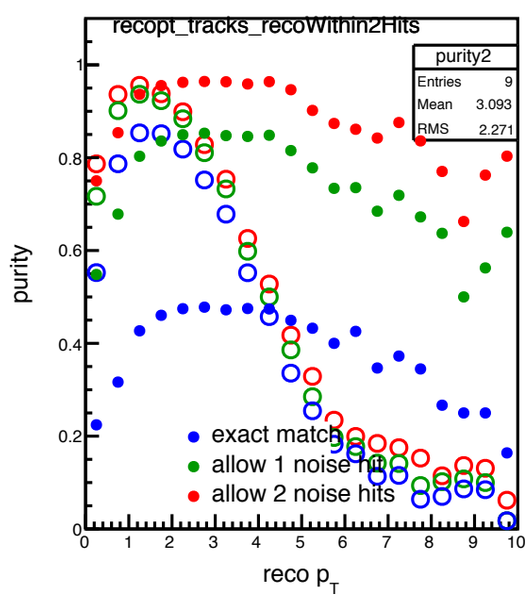


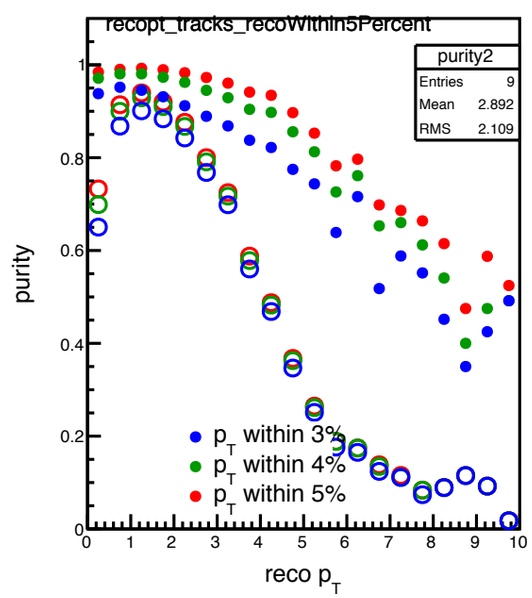










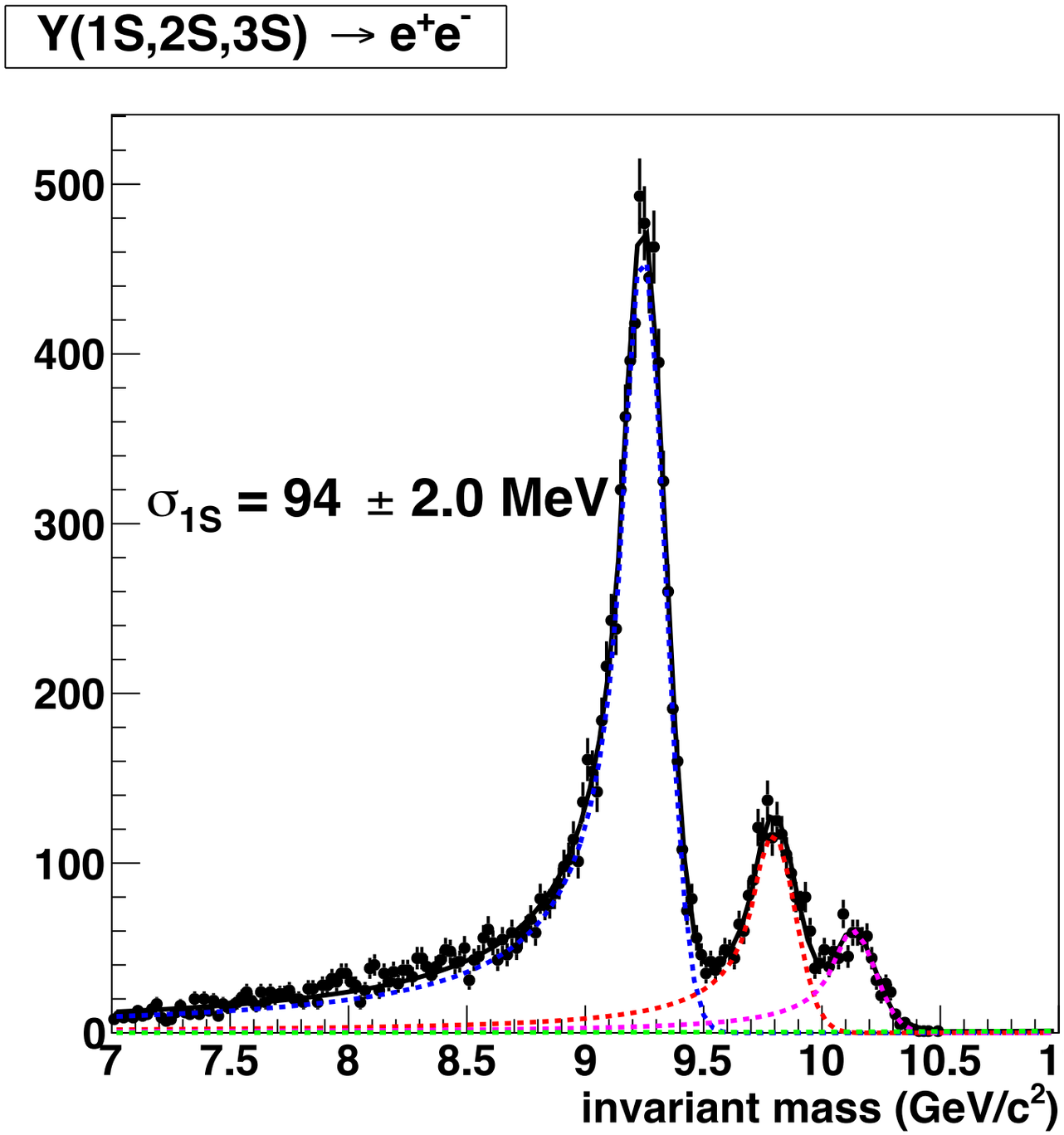


due to only one pixel layer

Can allowing poor efficiency recover purity?

Single upsilon

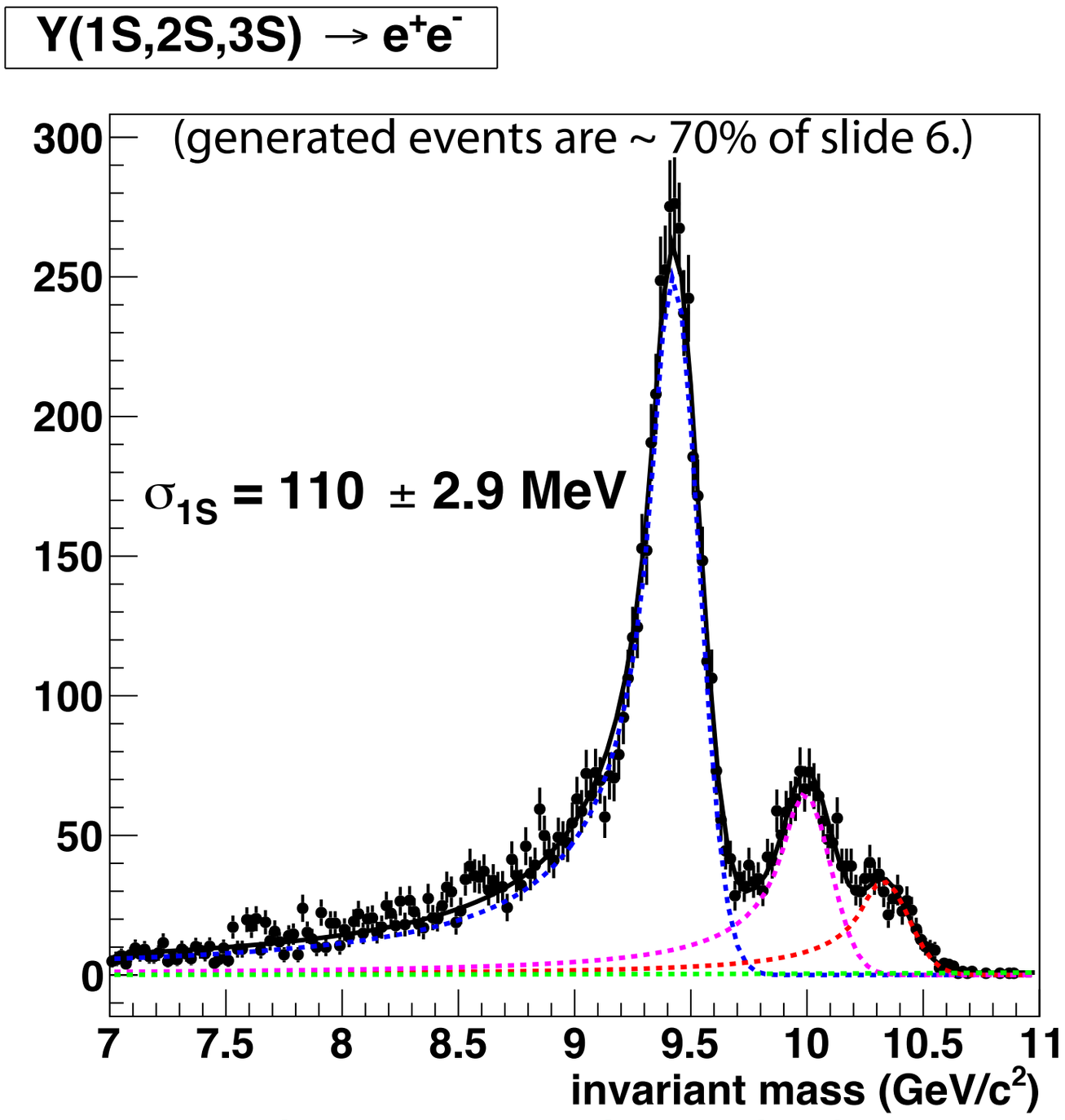
Single upsilon 1S/2S/3S with internal bremsstrahlung.



Upsilon mass resolution looks OK.

Upsilon embedded in central HIJING

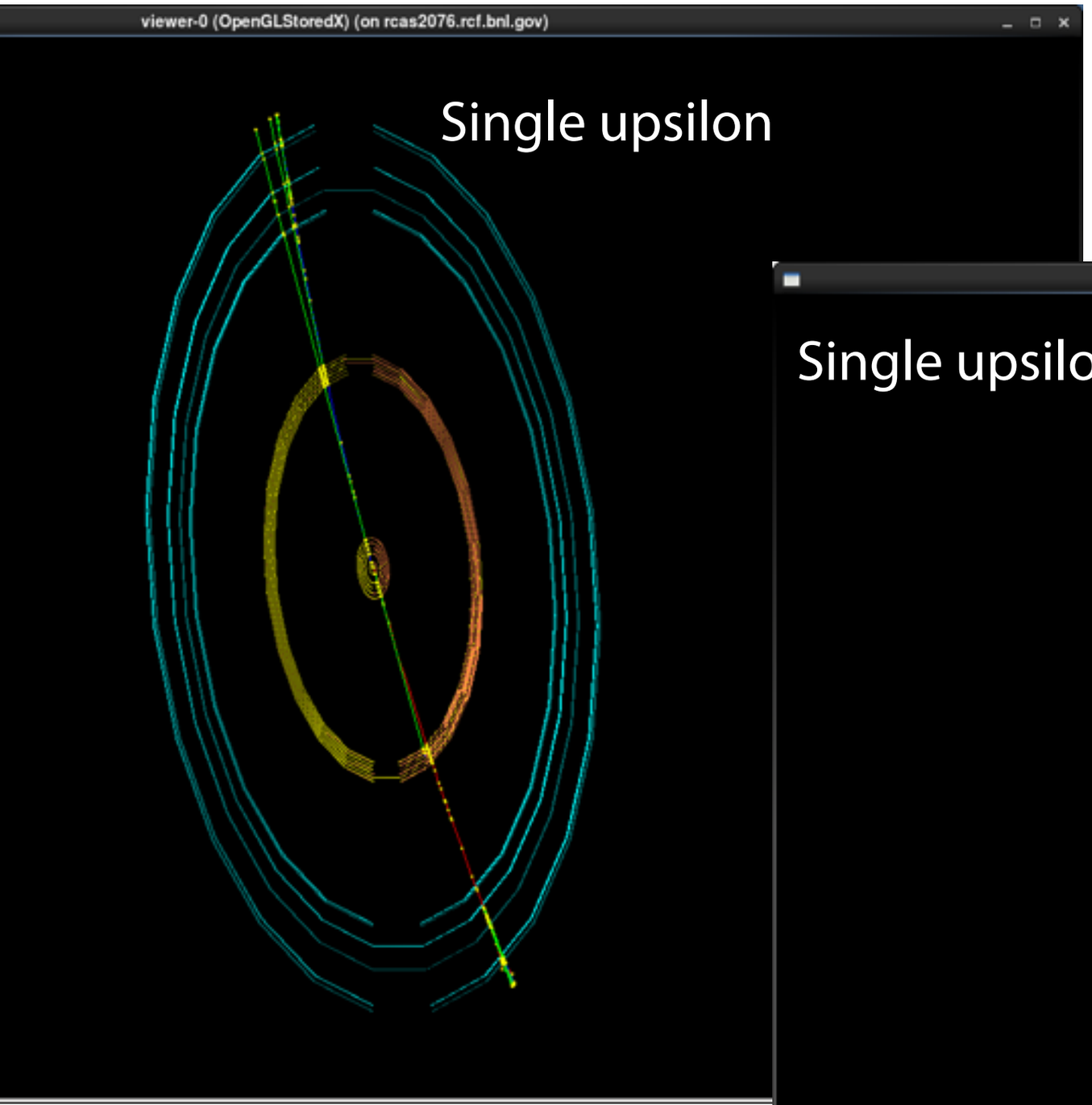
Single upsilon 1S/2S/3S with internal bremsstrahlung embedded in central HIJING



Upsilon mass resolution looks OK.

Event display

Single upsilon forced to decay into e+e- at η = 0.
|dz| < 0.5 cm corresponds to the strip size along z dir.



(slice at |dz| < 0.5 cm)

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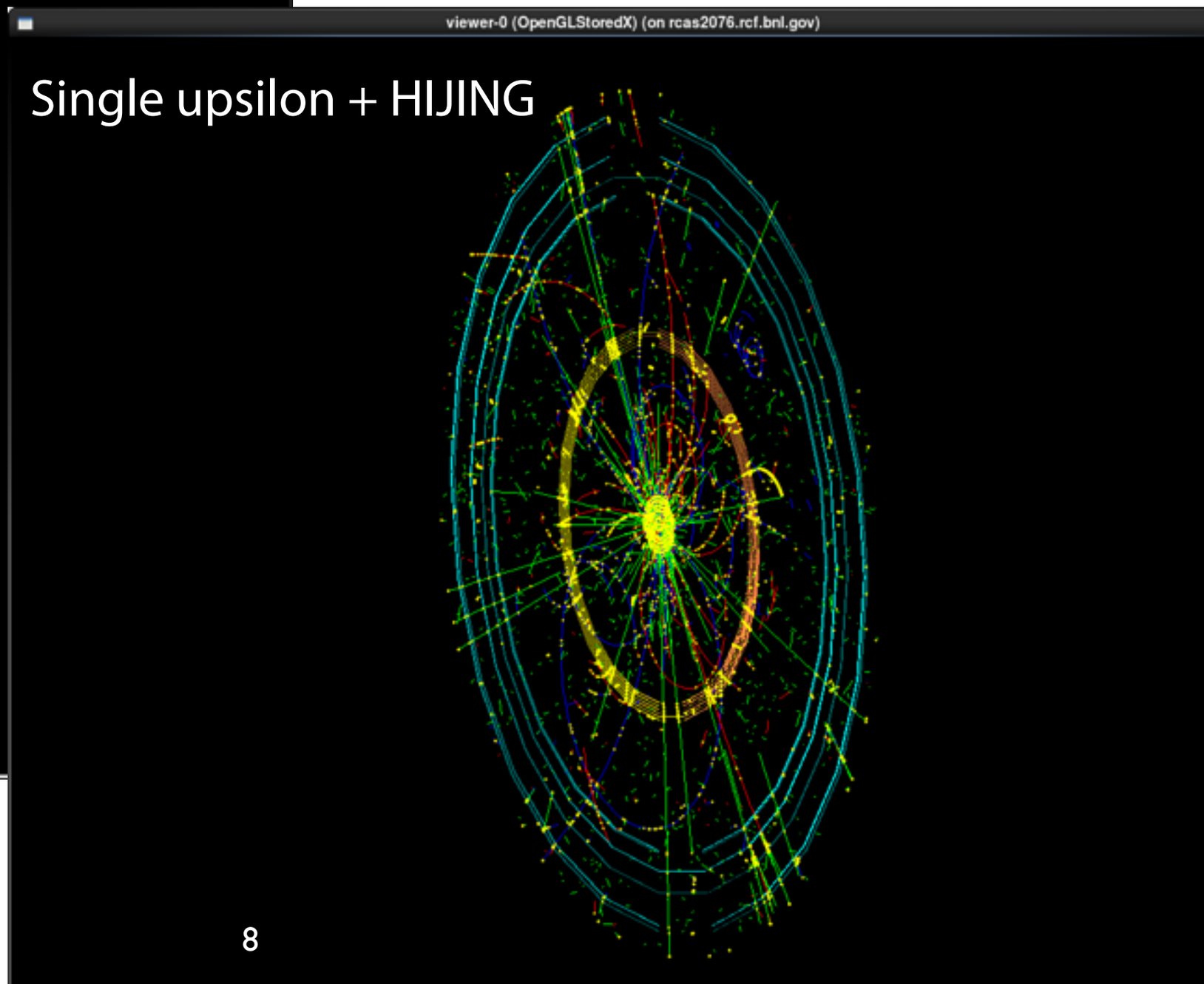

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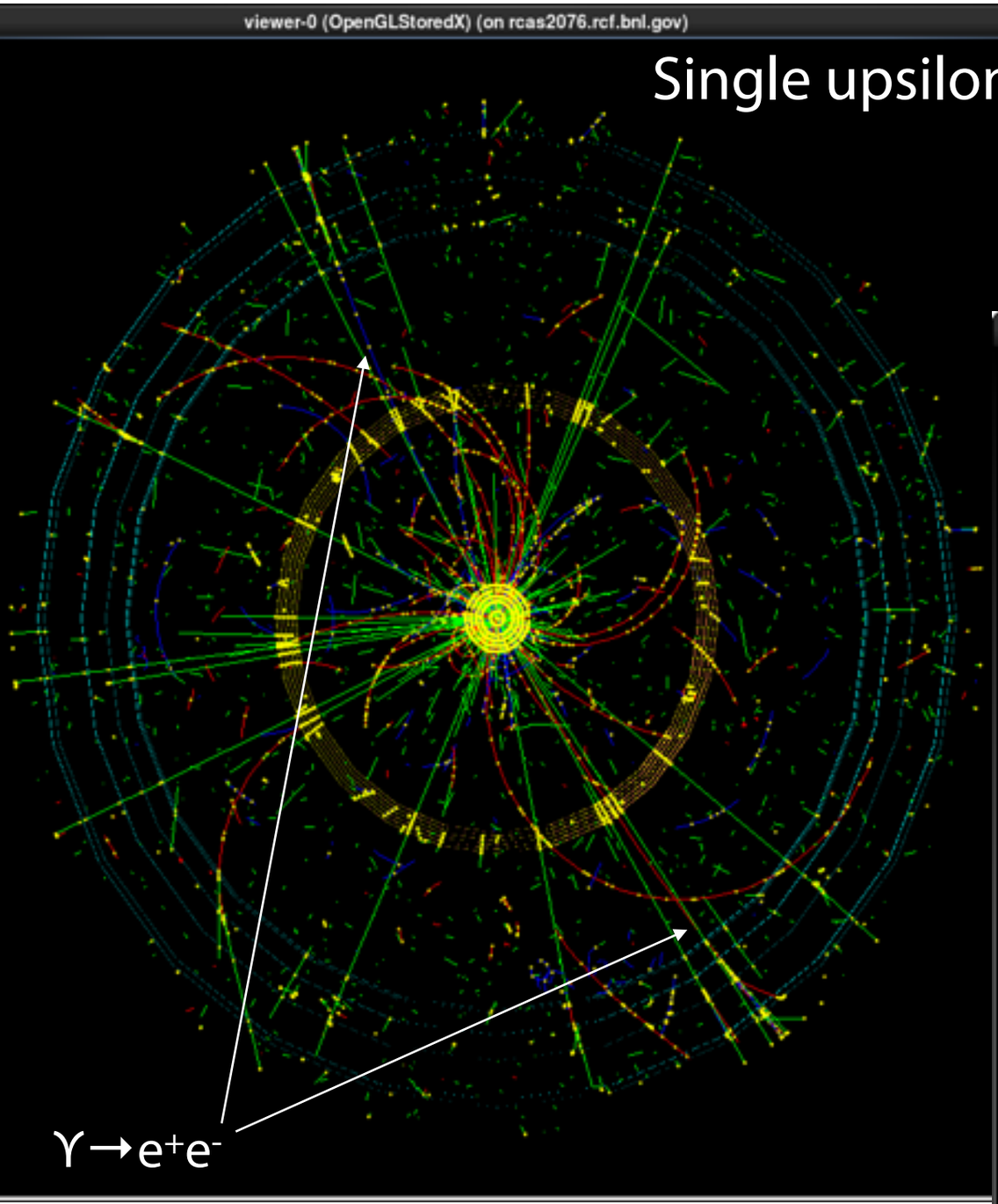

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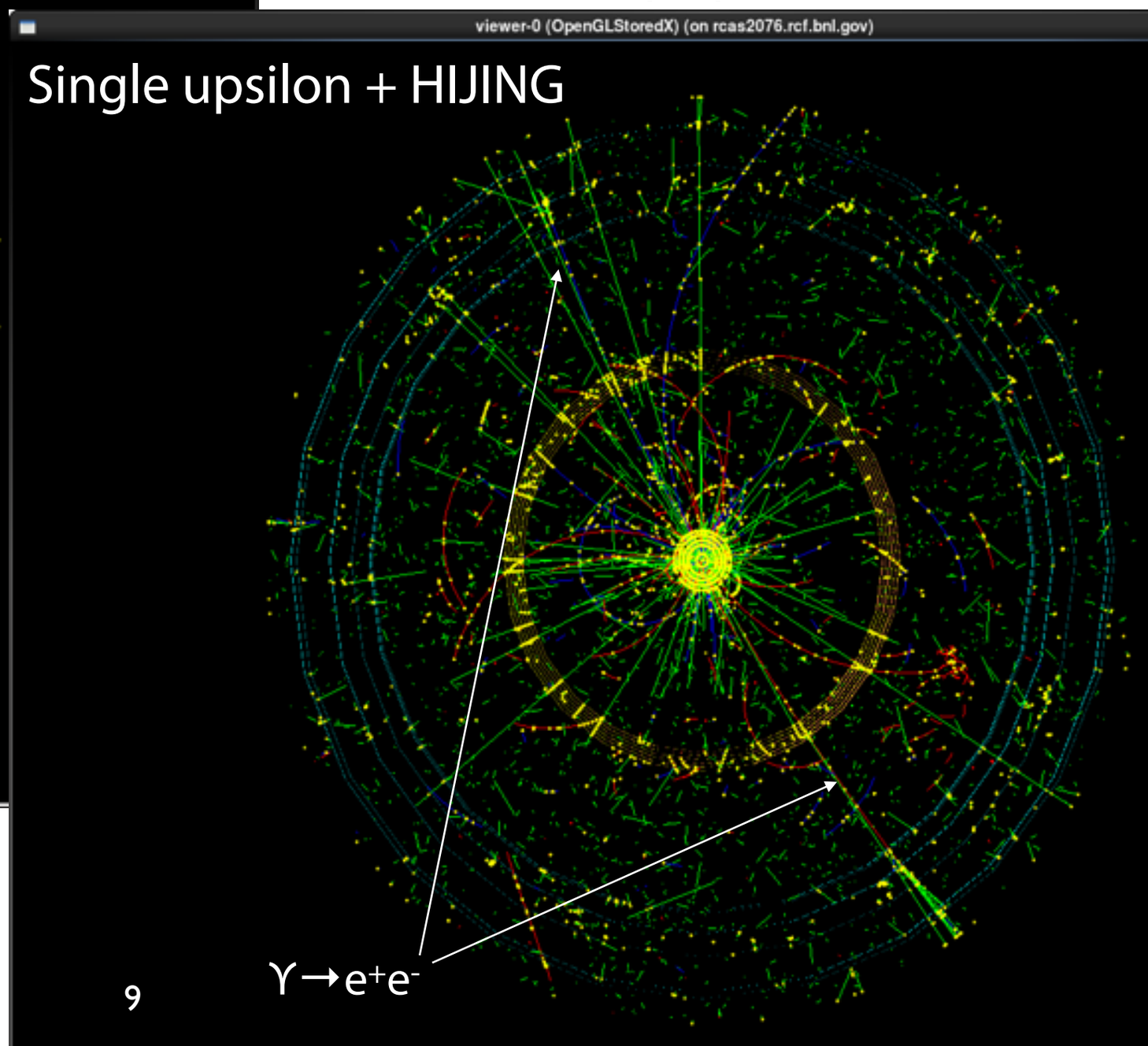


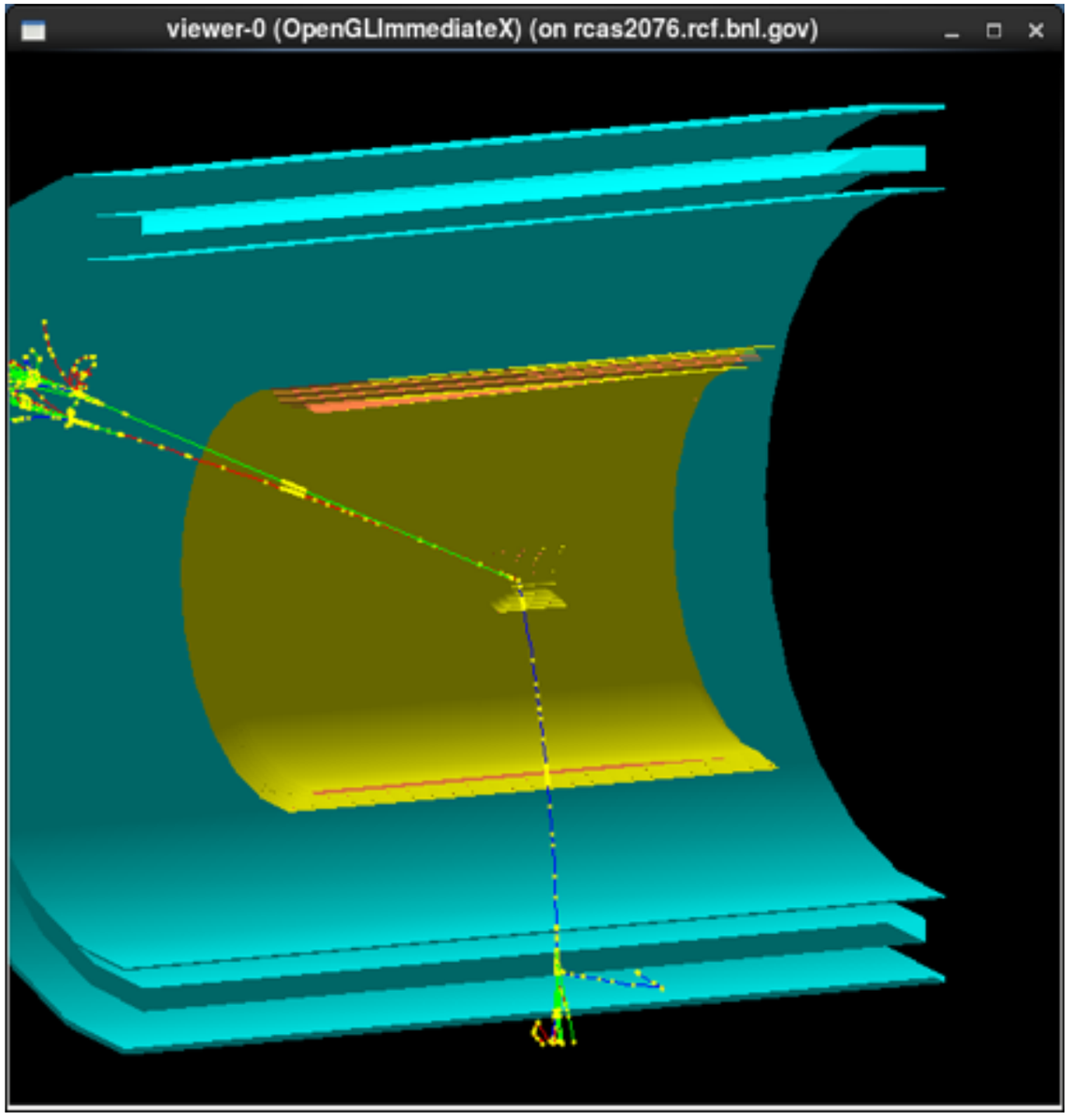
Summary

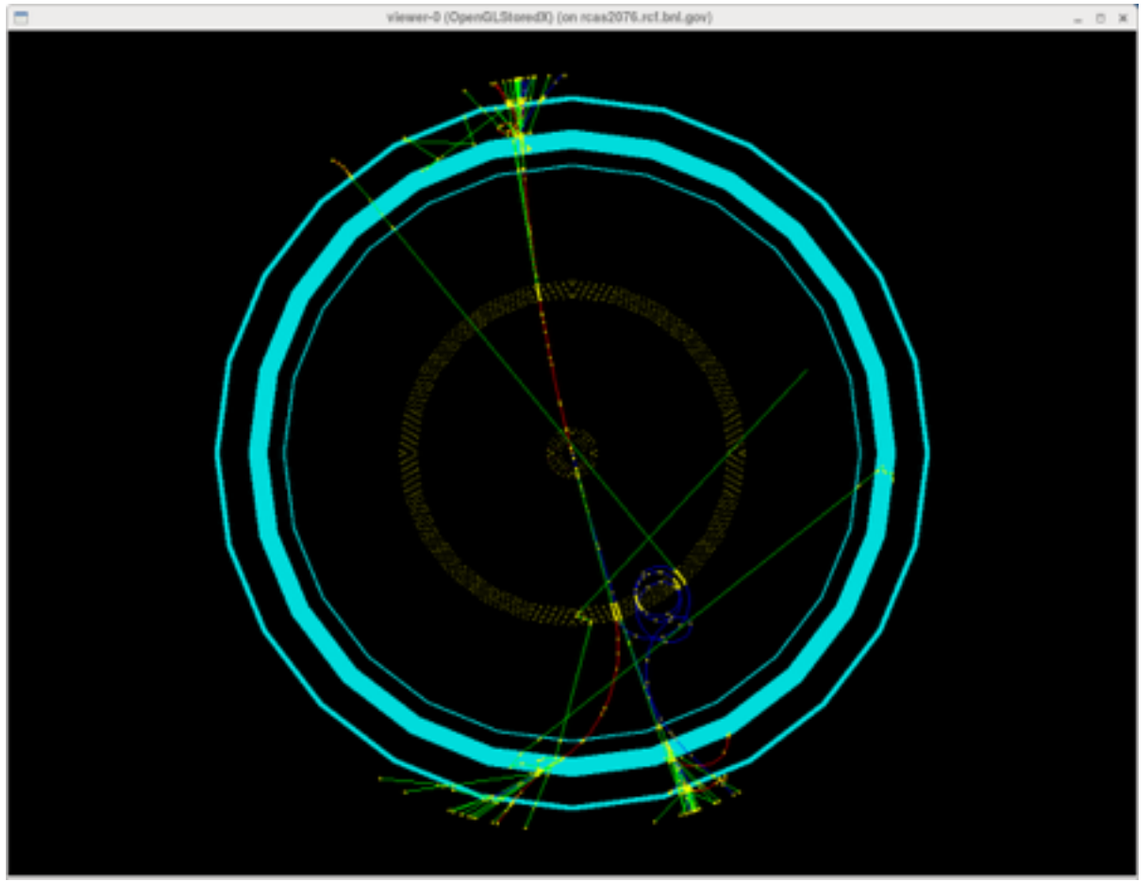
- G4 simulations indicate that intermediate tracker (4points) + thiner outer tracker (6 points) combination works for upsilon measurements.
  - single upsilon: σ(1S) = 94 +/- 2.0 MeV/c
  - single upsilon embed in central HIJING: σ(1S) = 110 +/- 2.9 MeV/c.

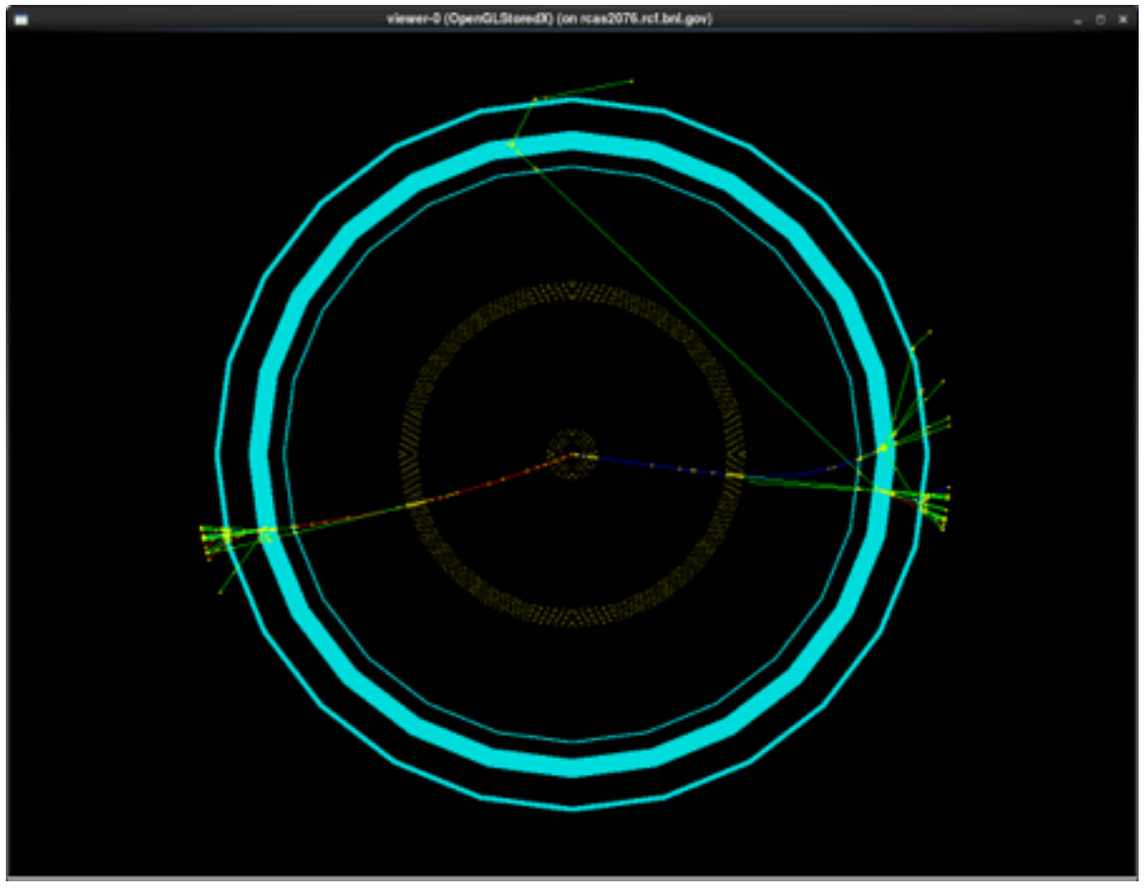
- Need to study
  - an impact of this combination on jet physics
  - reduction of track ambiguity in a large pileup probability.

Backup

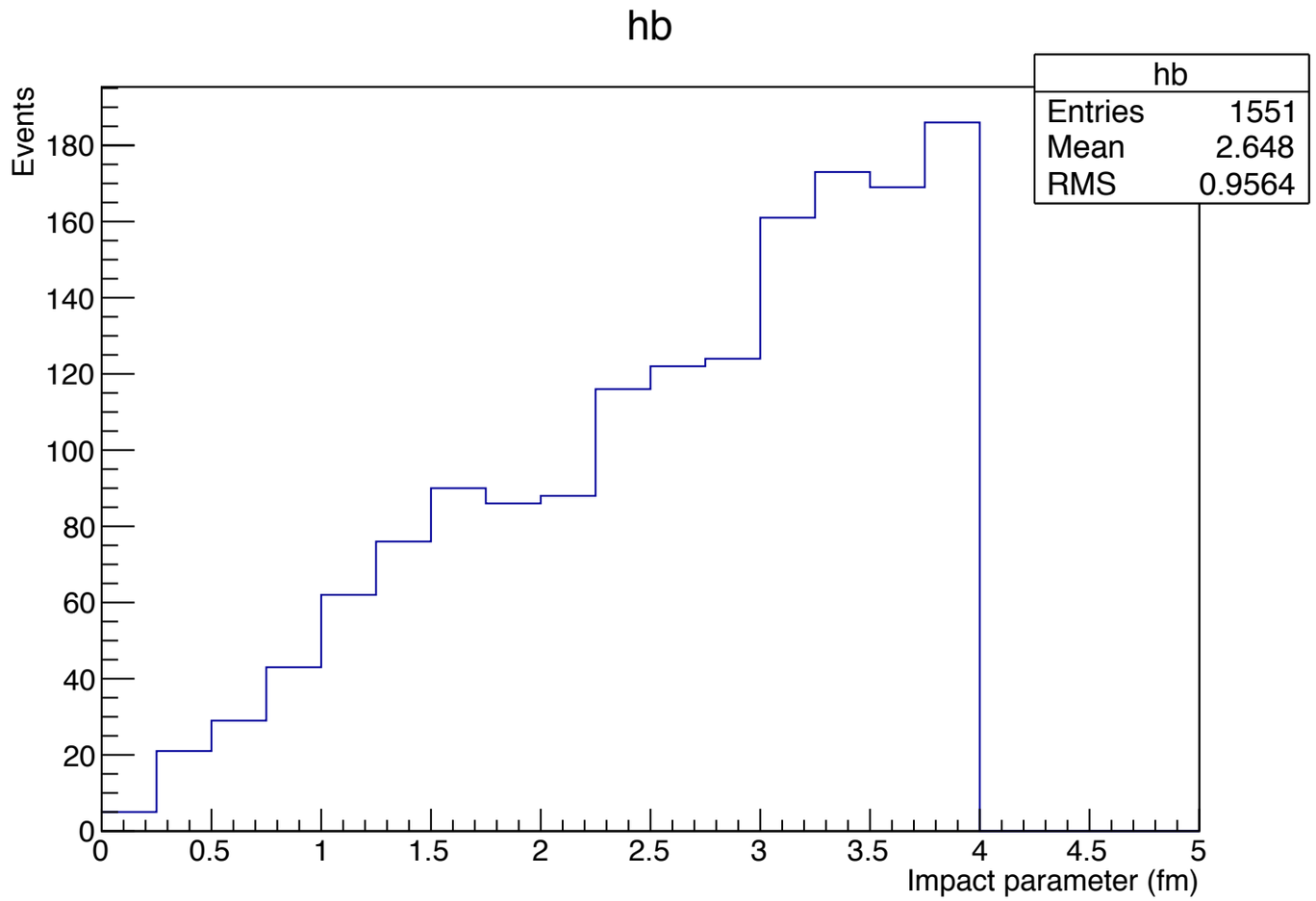
Event display



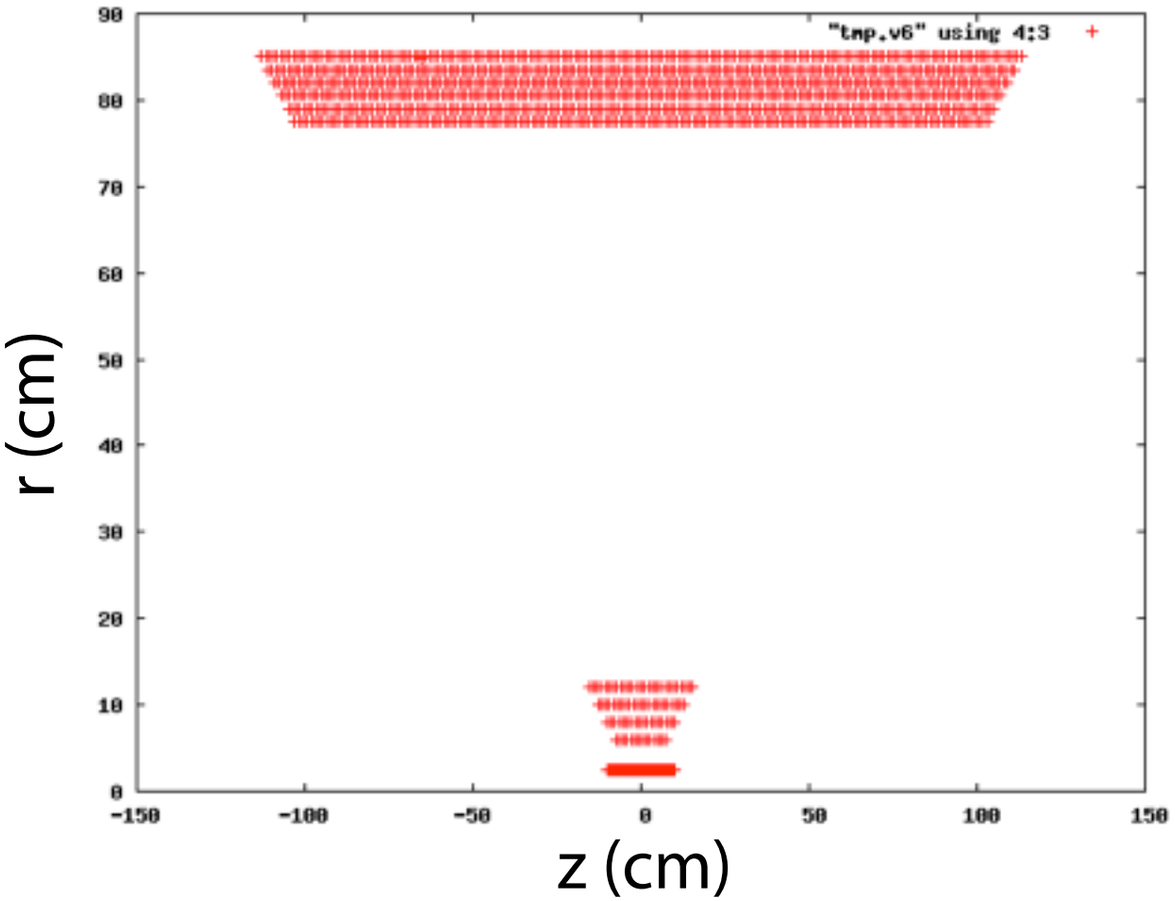


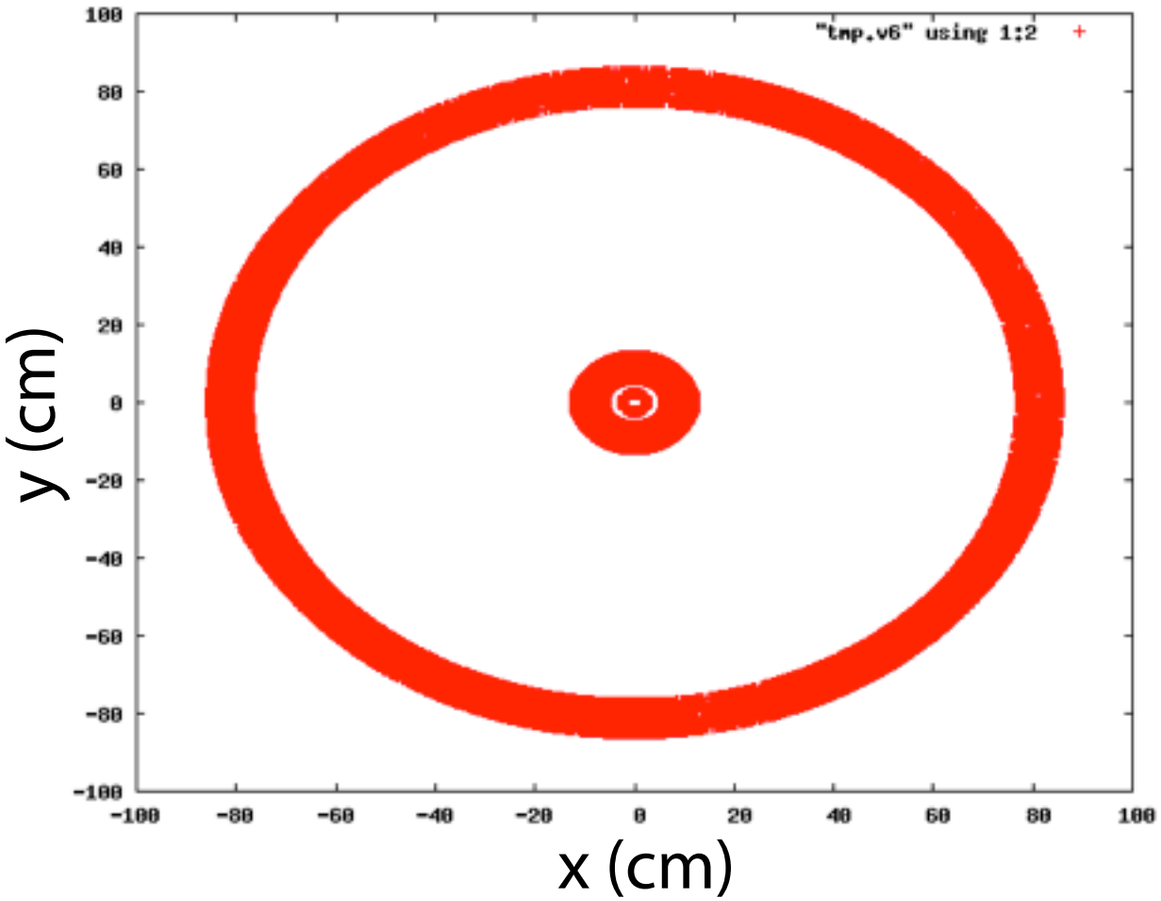


Impact parameter distribution



2D profile


"tmp.v6" using 4:3
r (cm)
z (cm)
90
80
70
60
50
40
30
20
10
0
-150
-100
-50
0
50
100
150


"tmp.v6" using 1:2
y (cm)
x (cm)
100
80
60
40
20
0
-20
-40
-60
-80
-100